Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	2	"09078872".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/13 09:36
S2	2	"09078872"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/13 09:37
S3	1	"09/078872"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/13 09:37
S4	2	"6173419".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/13 09:53
S5	2	"5228039".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/13 10:27
S6	3	(in adj circuit adj emulator) and (fpga same pod)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/13 10:35
S7	0	(fpga same microcontroller same lock$step)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/13 10:35
S8	0	(fpga same dut same lock$step)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/13 10:36
S9	1	(fpga same dut) and lock$step	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/13 10:36

S10	6	(fpga same microcontroller) and lock$step	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/13 10:36
S11	3	703/28.ccls. and lock$step	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/13 10:39
S12	386	(target adj (device microcontroller)) and fpga	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/13 10:39
S13	20	S12 and lock$step	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/13 10:40
S14	11	S13 and emulat$9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/13 10:41
S15	36	(fpga same interface) and (microcontroller same emulat$5)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/13 10:51
S16	0	(microcontroller and fpga and pod) and (co$simulation)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/13 10:51
S17	0	(microcontroller and fpga and pod) and (co$verification)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/13 10:51
S18	0	(microcontroller and pod) and (co$verification)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/13 10:51
S19	0	(microcontroller and pod) and (co$simulation)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/13 10:52

S20	18	(fpga and pod) and (co$simulation)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/13 10:54
S21	2	tzori.in. and emulator	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/13 10:59
S22	22	(pod and debugger and fpga)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/13 11:06
S23	367	(fpga same access) and microcontroller	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/13 11:06
S24	4	(fpga same visibility) and microcontroller	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/13 11:08
S25	124	(fpga same access same microcontroller)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/13 11:07
S26	1	S25 and "703".clas.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/13 11:08
S27	7	S25 and "714".clas.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/13 11:08
S28	1	pod same visibility same internal	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/13 11:09
S29	7	fpga same debugging same microcontroller	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/13 11:10

S30	3	(pod and ice and (fpga same interface))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/13 12:38
S31	1	(fpga same emulates same dut)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/13 12:39
S32	190	(fpga same (access visibility) same (dut microcontroller target))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/13 12:39
S33	0	S32 and pod	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/13 12:39
S34	42	S32 and emulat$5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/13 12:40
S35	15	S34 and "703".clas.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/13 12:40